Please add the following new claims:

10. (New) The semiconductor device of claim 1, wherein the inner signal line of the coaxial line has a thickness greater than a thickness of wiring layers in the functional blocks.

11. (New) The semiconductor device of claim 3, wherein the signal line has a thickness greater than a thickness of wiring layers in the functional blocks.

REMARKS

This is in response to the Office Action dated March 14, 2003. New claims 10-11 have been added. Thus, claims 1-5 and 10-11 are now pending. Attached hereto is a marked-up version of the changes made to the claim(s) by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"

Claim 3

Claim 3 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Ball. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 3 requires a "semiconductor device for transmitting a signal of high frequency of several GHz or more, the semiconductor device comprising: regions for forming a plurality of functional blocks; and a region for forming wiring layers for connecting the functional blocks, wherein each of the regions for forming the functional

blocks includes a multilayer wiring, and the region for forming the wiring layers for connecting the functional blocks includes a transmission line comprising a signal line for transmitting the signal of high frequency of several GHz or more, and ground lines and/or power source lines formed above and below the signal line, respectively, as viewed cross sectionally, to sandwich the signal line via an insulating film." See the instant specification at page 3, lines 11-24 for an example discussion of signals of several GHz or more.

The invention of claim 3 relates to a semiconductor device including a plurality of functional blocks wherein an interblock region is provided for connecting the functional blocks. It is possible to provide a semiconductor device in which wiring layers are constituted so as to be capable of transmitting signals of high frequency of several GHz or more without largely increasing the number of manufacturing steps. In particular, for example, in claim 3 the "region for forming the wiring layers for connecting the functional blocks includes a transmission line comprising a signal line for transmitting the signal of high frequency of several GHz or more, and ground lines and/or power source lines formed above and below the signal line, respectively, as viewed cross sectionally, to sandwich the signal line via an insulating film." A signal of high frequency is greatly influenced by interference from components of a semiconductor device. In order to reduce this interference, ground and/or power source line(s) are provided above and below the signal line (e.g., wee Fig. 3(3)).

In contrast to claim 3, Ball is directed to a technique for shielding a signal line provided *between* a plurality of IC chips (e.g., col. 1, lines 60-62) – not in a single

semiconductor device as in claim 3. In other words, Ball is directed to a technique for connecting a plurality of semiconductor devices. The invention of claim 3, on the other hand, requires that the functional blocks and interblock region be provided in the same semiconductor device. Ball is entirely unrelated to a wiring formed in a single semiconductor device, and fails to disclose or suggest the invention of claim 3 in this respect. Claim 3 is not anticipated by Ball; and is not rendered obvious since Ball teaches directly away from the invention of claim 3.

Claim 1

Claim 1 stands rejected under Section 103(a) as being allegedly unpatentable over Ball in view of Sim. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Ball and Sim are not properly combinable. In particular, as explained above, Ball relates to a technique for shielding a signal line provided *between* a plurality of IC chips (e.g., col. 1, lines 60-62) – not in a single semiconductor device as in claim 1. In other words, Ball is directed to a technique for connecting a plurality of semiconductor devices. In contrast, Sim is directed to a wiring formed in a single semiconductor device, and thus a different field of art from Ball. One of ordinary skill in the art would never have used Sim's single semiconductor wiring techniques in a system of Ball used for interconnected many chips, as the two are unrelated The Section 103(a) combination is legally improper for at least this reason.

Furthermore, claim 1 requires that the semiconductor device transmit a signal(s) of high frequency of several GHz or more. Sim clearly fails to disclose or suggest this

aspect of claim 1. Memory devices such as those of Sim process clock signals much lower in frequency than the high frequency signal(s) required by claim 1. Thus, even if the two references were combined as alleged in the Office Action, the invention of claim 1 still would not be met.

Claim 5

Claim 5 defines over the cited art for the reasons set forth above with respect to claim 1.

Moreover, claim 5 requires that "the region for forming the wiring layers for connecting the functional blocks includes wiring layers thicker than those in the functional blocks." For example, see Figs. 10-11 where the wiring layer(s) for connecting the functional blocks (see Figs. 10(B-3) and 11(B-5)) are thicker than the wiring of the functional blocks (see Figs. 10(A-3) and 11(A-5)). None of the three cited references disclose or suggest this aspect of claim 5. This clearly would not have been obvious in view of the cited art since no cited reference discloses or suggests such a feature. Accordingly, it can be seen that claim 5 patentably defines over the cited art.

Claims 10-11

Claims 10-11 also require that the signal line has a thickness greater than a thickness of wiring layers in the functional blocks. Again, the cited art fails to disclose or suggest this aspect of claims 10-11.

Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are now in condition for allowance. If any minor matter remains

to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Amended) A semiconductor device for transmitting a signal of high frequency of several GHz or more, the semiconductor device comprising:

regions for forming a plurality of functional blocks;

a region for forming wiring layers for connecting the functional blocks,

wherein each of the regions for forming the functional blocks includes a multilayer wiring, and

wherein the region for forming the wiring layers for connecting adjacent functional blocks includes a coaxial line comprising an inner signal line for transmitting the signal of high frequency of several GHz or more, and an outer ground line surrounding the signal line via an insulating film as viewed cross sectionally, so that the inner signal line and outer ground line have a common axis along at least a portion of a length of the coaxial line.

2. (Unamended) A semiconductor device according to claim 1, wherein a bottom surface of a wiring in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the coaxial line provided in the region for forming the wiring layers for connecting the functional blocks.

3. (Amended) A semiconductor device for transmitting a signal of high frequency of several GHz or more, the semiconductor device comprising:

regions for forming a plurality of functional blocks; and

a region for forming wiring layers for connecting the functional blocks,

wherein each of the regions for forming the functional blocks includes a multilayer wiring, and the region for forming the wiring layers for connecting the functional blocks includes a transmission line comprising a signal line for transmitting the signal of high frequency of several GHz or more, and ground lines and/or power source lines formed above and below the signal line, respectively, as viewed cross sectionally, to sandwich the signal line via an insulating film.

4. (Unamended) A semiconductor device according to claim 3, wherein a bottom surface of a wiring layer in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the ground line or power source line located below the transmission line provided in the region for forming the wiring layers for connecting the functional blocks.

5. (Amended) A semiconductor device for transmitting a signal of high frequency of several GHz or more, the semiconductor device comprising:

regions for forming a plurality of functional blocks;

a region for forming wiring layers for connecting the functional blocks,

wherein each of the regions for forming the functional blocks includes a multilayer wiring, and

wherein the region for forming the wiring layers for connecting the functional blocks includes wiring layers thicker than those in the functional blocks, and a bottom surface of a wiring layer in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the wiring layer provided in the region for forming the wiring layers for connecting the functional blocks as viewed cross sectionally.

Please add the following new claims:

10. (New) The semiconductor device of claim 1, wherein the inner signal line of the coaxial line has a thickness greater than a thickness of wiring layers in the functional blocks.

11. (New) The semiconductor device of claim 3, wherein the signal line has a thickness greater than a thickness of wiring layers in the functional blocks.